Method of Forming a Dual Damascene Via by Using a Metal Hard Mask Layer

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a method of forming a dual damascene via, in particular to a method of forming a dual damascene via by using a metal hard mask layer to prevent the via being connected with others vias to cause the leakage defects after forming the shape of the via.

2. Description of the Prior Art

In the manufacturing of devices on a semiconductor wafer, it is now the practice to fabricate multiple levels of conductive (typically metal) layers above a substrate. The multiple metallization layers are employed in order to accommodate higher densities as device dimensions shrink well below the one-micron design rules. Likewise, the size of inter-connective structures will also need to shrink, in order to accommodate the smaller dimensions. Thus, as integrated circuit technology advances into the sub-0.25 micron range, more advanced inter-connective architecture and new materials are required.

One such architecture is a dual damascene integration scheme in which a dual damascene structure is employed. The dual damascene process offers the advantage in process simplification by reducing the

process steps required to form the vias and trenches for a given metallization level. The openings, for the wiring of a metallization level and the underlying via connecting the wiring to a lower metallization level, are formed at the same time. The procedure provides an advantage in lithography and allows for improved critical dimension control. Subsequently, both the via and the trench can be filled utilizing the same metal-filling step, thereby reducing the number of processing steps required. Because of the simplicity of the dual damascene process, newer materials can cost-effectively replace the use of the existing aluminum (Al)/SiO_2 (silicon dioxide) scheme.

Referring to Fig. 1, this shows a diagram in forming the shape of the dual damascene via by using the traditional method. When the dual damascene via is formed by using the traditional method, a wafer, which comprises the first metal layer 10, a cap layer 20, the first low dielectric constant dielectric layer 30, a middle etching stop layer 40, the second low dielectric constant dielectric layer 50, the first hard mask layer 60, and the second hard mask layer 70, is must provided at first. The second step is to decide a location of an isolation layer on the second hard mask layer 70 and to form the second hard mask layer 70 on the isolation layer by using a photolithography and a etching procedure to remove the partial second hard mask layer 70. The third step is to form the first trench in the second low dielectric constant dielectric layer 50 and the middle etching stop layer 40 by using the photolithography and the etching procedure to remove the partial middle etching stop layer 40 and the partial second low dielectric constant dielectric layer 50. The fourth step is to form the second trench in the first low dielectric constant dielectric layer 30 and the cap layer 20 by using the photolithography

and the etching procedure to remove the partial first low dielectric constant dielectric layer 30, the partial middle etching stop layer 40, and the partial cap layer 20. The first trench and the second trench can be connected with each other to become the shape of the dual damascene via. The isolation layer, which is used to isolate the dual damascene via, is combined by using the middle etching stop layer 40, the second low dielectric constant dielectric layer 50, the first hard mask layer 60, and the second hard mask layer 70.

Referring to Fig. 2, after forming the shape of the dual damascene via on the wafer, a metal layer 80 is formed in the dual damascene via and filled of the dual damascene via. Then the surface of the wafer will become a planar surface by proceeding a chemical mechanical polishing procedure and the dual damascene via procedure is finished.

In the traditional dual damascene via procedure, in order to prevent the first low dielectric constant dielectric layer 30 and the second low dielectric constant dielectric layer 50 being affected by the stress, which is produced in the chemical mechanical polishing procedure, to cause the deformation defect or contacting with the slurry directly to change properties of the first low dielectric constant dielectric layer 30 and the second low dielectric constant dielectric layer 50, there are one to three dielectric layers must being formed on the second low dielectric constant dielectric layer 50 to eliminate the influence of the stress and to avoid the changes of the properties. These one to three dielectric layers are the first hard mask layer 60 and the second hard mask layer 70. But in the present procedure, the selective etching rate

among the first hard mask layer 60, the second hard mask layer 70, the first low dielectric constant dielectric layer 30, and the second low dielectric constant dielectric layer 50 is not enough. Therefore, the first hard mask layer 60 and the second hard mask layer 70 will usually have the rounding profile after finishing the etching procedures from the second step to the fourth step. This rounding profile will decrease the distance between the dual damascene vias and decrease the process window in the back-end chemical mechanical polishing procedure. This rounding profile will also produce the bridging defect between the dual damascene vias more easily to cause the leakage defect. This rounding profile will further decrease the qualities of the semiconductor device and will increase the cost of the procedure.

SUMMARY OF THE INVENTION

In accordance with the background of the above-mentioned invention, the traditional method will produce the rounding profile on the surface of the isolation layer easily to affect the process window of the back-end procedure and to produce the bridging defect between the dual damascene vias easily to cause the leakage defect. The present invention provides a method of forming the dual damascene via by using the metal layer to be the hard mask layer to make the surface of the isolation layer, which is between the dual damascene vias, become a level and smooth surface to avoid the bridging defect, which is produced between the dual damascene vias.

The second objective of this invention is avoid the leakage defect, which is produced between the dual damascene vias, by using the metal

layer to be the hard mask layer to make the surface of the isolation layer, which is between the dual damascene vias, become a level and smooth surface.

The third objective of this invention is to increase the process window in the back-end procedure by using the metal layer to be the hard mask layer to make the surface of the isolation layer, which is between the dual damascene vias, become a level and smooth surface.

The fourth objective of this invention is to increase the qualities of the semiconductor device by using the metal layer to be the hard mask layer to make the surface of the isolation layer, which is between the dual damascene vias, become a level and smooth surface.

The further objective of this invention is to decrease the cost of the procedure by using the metal layer to be the hard mask layer to make the surface of the isolation layer, which is between the dual damascene vias, become a level and smooth surface.

In according to the foregoing objectives, the present invention provides a method of forming the dual damascene via by using the metal layer to be the hard mask layer to make the surface of the isolation layer, which is between the dual damascene vias, become a level and smooth surface to avoid the bridging defect, which is produced between the dual damascene vias. The present invention will also avoid the leakage defect, which is produced between the dual damascene vias and to increase the width of the procedure in the back-end procedure. The present invention will further increase the qualities of the semiconductor device and

decrease the cost of the procedure.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawing forming a material part of this description, there is shown:

Fig. 1 shows a diagram in forming the shape of the dual damascene via by using the traditional method;

Fig. 2 shows a diagram in filling of the dual damascene via, which is formed by using the traditional method, by a metal layer and proceeding a chemical mechanical polishing procedure;

Fig. 3 shows a diagram in forming a cap layer, the first low dielectric constant dielectric layer, the middle etching stop layer, the second low dielectric constant dielectric layer, dielectric hard mask layer, and the second metal layer on the first metal layer;

Fig. 4 shows a diagram in removing the partial second metal layer;

Fig. 5 shows a diagram in forming a bottom anti-reflective coating and a photo mask layer on the second metal layer and the partial dielectric hard mask layer and forming the first trench in the second low dielectric constant dielectric layer and the dielectric hard mask layer;

Fig. 6 shows a diagram in removing the bottom anti-reflective

coating and a photo mask layer;

Fig. 7 shows a diagram in removing the partial dielectric hard mask layer and the middle etching stop layer which is at the bottom of the first trench;

Fig. 8 shows a diagram in removing the partial first low dielectric constant dielectric layer and the partial second low dielectric constant dielectric layer to form the second trench in the second low dielectric constant dielectric layer and to form the third trench in the first low dielectric constant dielectric layer;

Fig. 9 shows a diagram in removing the middle etching stop layer, which is at the partial bottom of the second trench, and the cap layer, which is at the bottom of the third trench;

Fig. 10 shows a diagram in forming a barrier layer on the second metal layer, the sidewalls and the partial bottom of the second trench, and the sidewalls and the bottom of the third trench;

Fig. 11 shows a diagram in forming the third metal layer on the barrier layer and filling of the second trench and the third trench;

Fig. 12 shows a diagram in removing the partial third metal layer by using the chemical mechanical polishing procedure to expose the barrier layer, which is on the isolation layer;

Fig. 13 shows a diagram in removing the partial barrier layer to

expose the second metal layer, which is on the isolation layer; and

Fig. 14 shows a diagram in removing the second metal layer to expose the dielectric hard mask layer, which is on the isolation layer.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The foregoing aspects and many of the intended advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

One such newer material is copper. The use of copper metallization improves performance and reliability over aluminum, but copper introduces additional problems that are difficult to overcome when using known techniques for aluminum. For example, in conventional aluminum inter-connective structures, a barrier layer is usually not required between the aluminum metal line and an SiO_2 inter-level dielectric (ILD). However, when copper is utilized, copper must be encapsulated from the surrounding ILD, since copper diffuses/drifts easily into the adjoining dielectric. Once the copper reaches the silicon substrate, it will significantly degrade the device's performance.

In order to encapsulate copper, a barrier layer of some sort is required to separate the copper from the adjacent material(s). Because copper encapsulation is a necessary step requiring a presence of a

barrier material to separate the copper, other materials can now be substituted for the SiO_2 as the material for ILD. Replacing the SiO_2 by a low-dielectric constant material reduces the interline capacitance, thereby reducing the resistance capacitance (RC) delay, cross-talk noise and power dissipation in the inter-connective place. However, it is generally necessary to have a barrier (or liner) present between the inter-connective place and the low dielectric constant ILD to prevent possible interaction between the inter-connective place and the low-dielectric constant ILD and also to provide adhesion between them. This barrier is desirable even when aluminum is utilized for the inter-connective place.

Referring to Fig. 3, a wafer must be provided at first and the wafer comprises the first metal layer 100. Then a cap layer 200 is formed on the first metal layer 100 and the first low dielectric constant dielectric layer 300 is formed on the cap layer 200. The cap layer 200 is formed by using the chemical vapor deposition (CVD) procedure and the material of the cap layer 200 is silicon nitride (SiN) or silicon carbon (SiC). The thickness of the cap layer 200 is about 100 to 1000 angstroms. The low dielectric constant material, such as: oxide or fluorinated silicon dioxide (FSG), is most used to be the material of the first low dielectric constant dielectric layer 300. The thickness of the first low dielectric constant dielectric layer 300 is about 1000 to 5000 angstroms. Then a middle etching stop layer 400 is formed on the first low dielectric constant dielectric layer 300 and the second low dielectric constant dielectric layer 500 is formed on the middle etching stop layer 400. Silicon nitride or silicon carbon is most used to be the material of the middle etching stop layer 400 and the low dielectric constant material, such as: oxide or

fluorinated silicon dioxide (FSG), is most used to be the material of the second low dielectric constant dielectric layer 500. The thickness of the middle etching stop layer is about 100 to 1000 angstroms and the thickness of the second low dielectric constant dielectric layer 500 is about 1000 to 5000 angstroms. At last, a dielectric hard mask layer 600 is formed on the second low dielectric constant dielectric layer 500 and the second metal layer 700 is formed on the dielectric hard mask layer 600. Silicon nitride or silicon carbon is most used to be the material of the dielectric hard mask layer 600. The second metal layer 700 is used to be a metal hard mask layer and is formed by using the chemical vapor deposition procedure or the physical vapor deposition procedure. Titanium, titanium nitride, tantalum, tantalum nitride, aluminum, or tungsten is most used to be the material of the second metal layer 700. The thickness of the dielectric hard mask layer 600 is about 100 to 1000 angstroms and the thickness of the second metal layer 700 is about 50 to 500 angstroms.

Referring to Fig. 4, after deciding the location of the isolation layer on the second metal layer 700, the partial second metal layer 700 is removed by using the photolithography and the etching procedure to form the second metal layer 700 on the isolation layer and expose the partial dielectric hard mask layer 600. Referring to fig. 5, after deciding the location of the first trench 710 on the dielectric hard mask layer 600, a bottom anti-reflective coating 800 and a photo mask layer 810 are formed on the second metal layer 700 and the exposed dielectric hard mask layer. Following the needs of the procedure, sometimes the bottom anti-reflective coating 800 and the photo mask layer 810 may be omitted to increase the proceeding efficiency of the procedure. Then the partial

dielectric hard mask layer 600 and the partial second low dielectric constant dielectric layer 500 are removed by using the photolithography and the etching procedure to form the first trench 710 in the dielectric hard mask layer 600 and the second low dielectric constant dielectric layer 500. The middle etching stop layer 400 is exposed at the bottom of the first trench 710. At last, the bottom anti-reflective coating 800 and the photo mask layer 810 are removed (referring to Fig. 6).

Referring to Fig. 7, the middle etching stop layer 400, which is at the bottom of the first trench 710, and the exposed dielectric hard mask layer 600 are removed by using the etching procedure after deciding the location of the second trench. The dielectric hard mask layer 600, which is on the isolation layer, will be protected by the second metal layer 700 and will not be removed in the etching procedure. Referring to Fig. 8, the partial second low dielectric constant dielectric layer 500 and the partial first low dielectric constant dielectric layer 300 are removed by using the etching procedure to form the second trench 720 in the second low dielectric constant dielectric layer 500, the dielectric mask layer 600, and the second metal layer 700 and to form the third trench 730 in the first low dielectric constant dielectric layer 300. The partial second trench 720 is connected with the third trench 730 to become the shape of the dual damascene via. The partial bottom of the second trench 720 exposes the middle etching stop layer 400 and the bottom of the third trench 730 exposes the cap layer 200.

Referring to Fig. 9, the middle etching stop layer 400, which is at the partial bottom of the second trench 720, and the cap layer 200, which is at the bottom of the third trench 730 are removed by the

etching procedure to expose the first low dielectric constant dielectric layer 300 at the partial bottom of the second trench 720 and to expose the first metal layer 100 at the bottom of the third trench 730. From Fig. 7 to Fig. 9, the properties of the second metal layer 700, which is used to be the metal hard mask layer, is different from the properties of the dielectric material, such as: dielectric hard mask layer 600, middle etching stop layer 400, the first low dielectric constant dielectric layer 300, and the second low dielectric constant dielectric layer 500, in the etching procedure. Therefore, the very high etching selective rate (>20) will be got among the second metal layer 700 and others dielectric materials in the etching procedure to make the surface of the second metal layer 700 become a level and smooth surface. This condition will avoid the surface of the second metal layer 700 to become the rounding profile because of the unenough etching selective rate.

Referring to Fig. 10, a barrier layer 850 is formed on the sidewalls and the partial bottom of the second trench 720, the sidewalls and the bottom of the third trench 730, and the second metal layer 700. Tantalum nitride/tantalum or titanium nitride/titanium is most used to be the material of the barrier layer 850. Referring to Fig. 11, the third metal layer 900 is formed on the barrier layer 850 and is filled in the second trench 720 and the third trench 730 to the full. Aluminum or copper is most used to be the material of the third metal layer 900. In the embodiment, copper is used to be the material of the third metal layer 900 and the scope of the present invention is not limited. The copper layer is deposited on the barrier layer 850 by using the copper electroplating procedure to be the third metal layer 900.

Referring to Fig. 12, the partial third metal layer 900 is removed by using the chemical mechanical polishing procedure to expose the barrier layer 850 on the isolation layer and to make the surface of the third metal layer 900 and the barrier layer 850 become a level and smooth surface. Because the present invention uses the second metal layer 700 to be the hard mask layer. Therefore, the process window of the chemical mechanical polishing procedure will be more enough and the bridging defect will not be produced at the place between the dual damascene vias to avoid the leakage defects. Referring to Fig. 13, the barrier layer 850 is removed by using the chemical mechanical polishing procedure or the etching procedure. Referring to Fig. 14, the second metal layer 700 is removed by using the chemical mechanical polishing procedure or the etching procedure and the dual damascene procedure is finished. The second metal layer 700 and the barrier layer 850 can be removed at the same time in the same procedure, such as: the chemical mechanical polishing procedure or the etching procedure.

In accordance with the present invention, the present invention provides a method of forming the dual damascene via by using the metal layer to be the hard mask layer to make the surface of the isolation layer, which is between the dual damascene vias, become a level and smooth surface to avoid the bridging defect, which is produced between the dual damascene vias. The present invention will also avoid the leakage defect, which is produced between the dual damascene vias and to increase the process window in the back-end procedure. The present invention will further increase the qualities of the semiconductor device and decrease the cost of the procedure.

Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from what is intended to be limited solely by the appended claims.